

ABSTRACT OF THE DISCLOSURE

A digitally implemented timing recovery circuit for recovering a clock
5 signal from an input bit stream. The recovery circuit comprising an edge detector
for detecting a transition from "0" to "1" or "1" to "0" in the input bit stream, a
phase counter having a plurality of registers indicative of the phase counter
transition state, and a loop counter having a plurality of registers indicative of the
10 loop counter transition state. When the phase counter reaches a particular
transition state, a recovered clock pulse is enabled. The phase counter is
preferably non-linear to optimize the circuit.

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